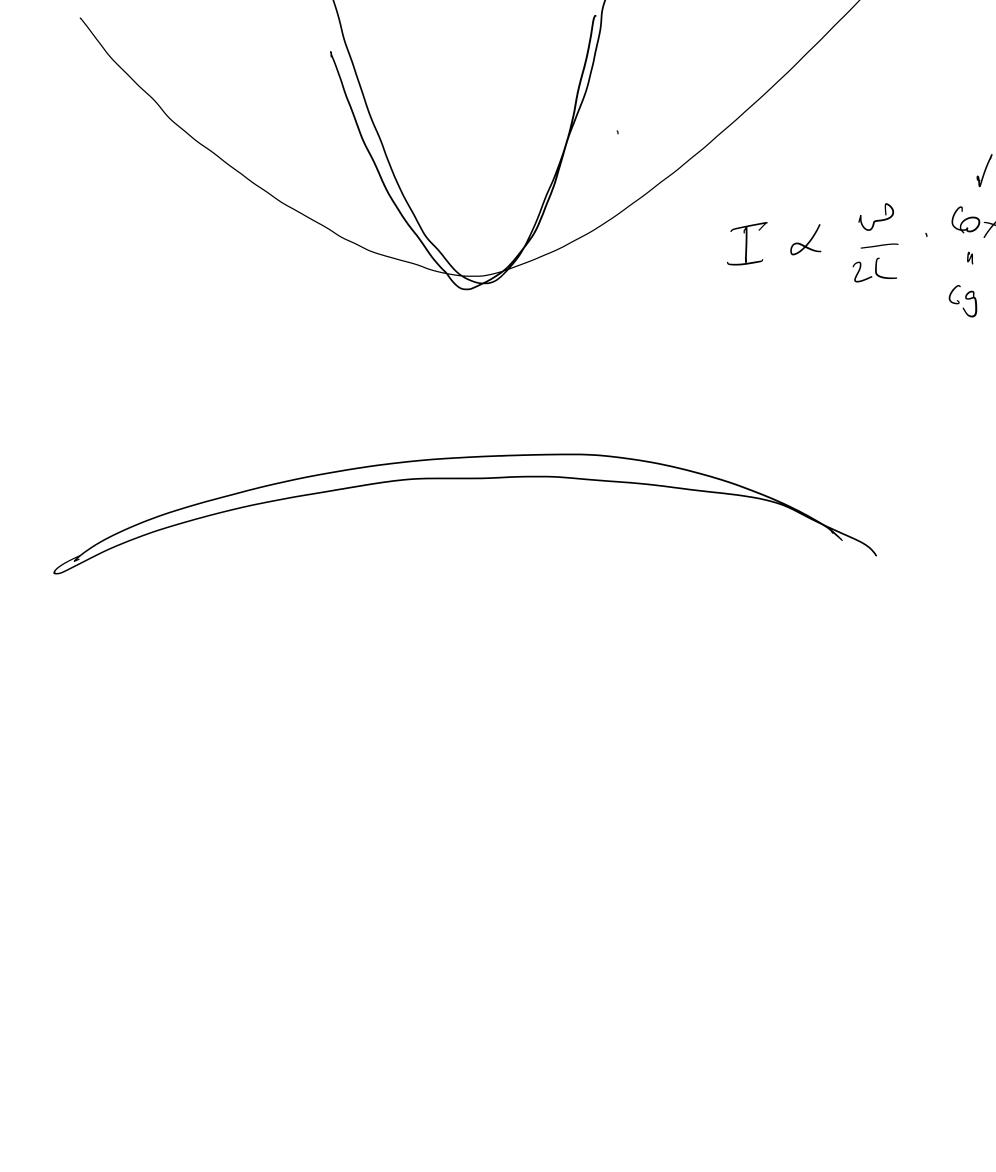
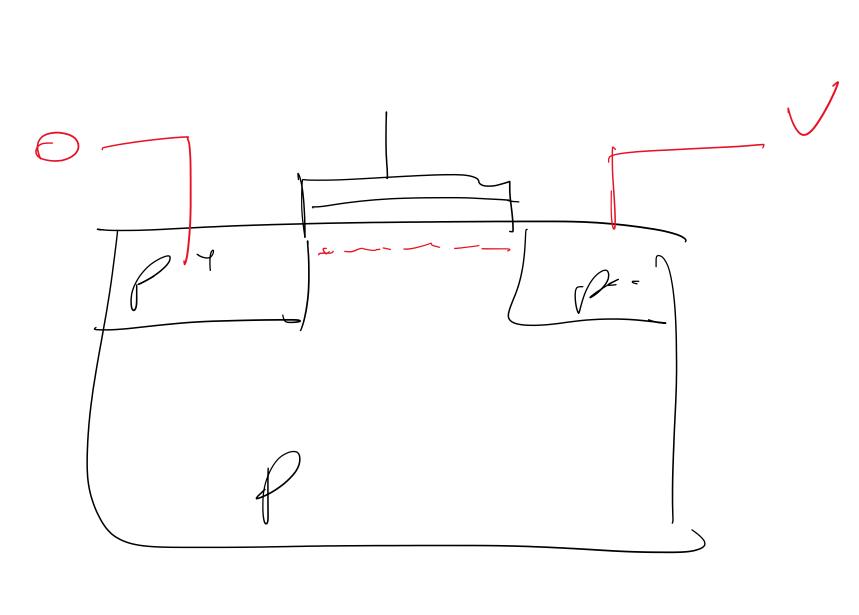
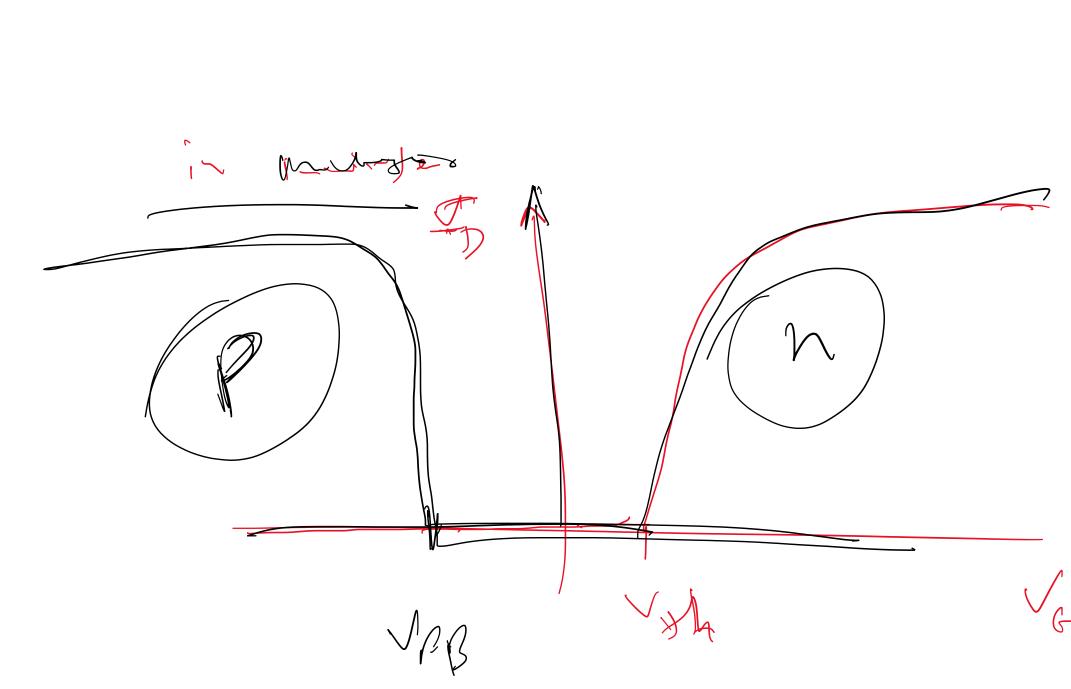
## Wednesday, 11 December 2024 10:11 ies 5\_EE557 ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE **EPFL** SCHOOL OF ENGINEERING (STI) Institute of Electrical Engineering (IEL) EE 557 - Principles of semiconductor devices Responsible: Prof. Elison Matioli Teaching assistant: Alessandro Floriduz: alessandro.floriduz@epfl.ch Exercises - list 5 1. Consider an MOS structure that consists of a n<sup>+</sup>-poly-Si gate, a 9 nm SiO<sub>2</sub> insulator, on a p-Si substrate with a doping level $N_A=3\times10^{17}$ cm<sup>-3</sup>. At room temperature and for $V_g=-3$ , 0, 0.3 and 3 V, compute numerical values for: a) the surface potential; b) the total charge per unit area in the semiconductor and its breakdown into electron charge and hole charge; c) the electric field in the oxide; d) the extension of the depletion region in the semiconductor; e) the low-frequency capacitance; f) the high-frequency capacitance. 2. Consider an MOS structure with a n<sup>+</sup>-Si gate on a p-type Si substrate characterized by the following parameters: $W_M = \chi_{Si} = 4.04 \text{ eV}$ , $x_{ox} = 9 \text{ nm}$ , $N_A = 1.2 \times 10^{17} \text{ cm}^{-3}$ , T=300K. For t < 0, a voltage $V_I = -2$ V has been applied from the gate to the bulk of the semiconductor for a long time. At t = 0, the applied voltage abruptly changes to $V_2 = 3$ V. a) Calculate the semiconductor charge and the electric field in the oxide at $t = 0^-$ . What regime is the MOS structure in? b) Calculate the semiconductor charge and the electric field in the oxide at $t = 0^+$ . Consider any RC delays negligible. What regime is the MOS structure in? c) Calculate the semiconductor charge and the electric field in the oxide for $t\rightarrow\infty$ . What regime is the MOS structure in? 3. Ionizing radiation has an adverse impact on MOSFETs: high energy particles (e.g. x-rays, gamma-rays, electrons, protons, etc...) going through the device will create hole-electron pairs (ionization effect). The situation is critical for the SiO<sub>2</sub> gate oxide: electrons in SiO<sub>2</sub> are relatively mobile (20 cm<sup>2</sup>/Vs) and can be readily collected by the gate metal; on the bq7 - 8: Ws 7Wm 1 +5 EF -2) $\Phi_{\text{rth}} = \frac{2k\tau}{q}$ , $\ln\left(\frac{N_2}{h_i}\right) = 0.89v$ $\delta = \frac{\sqrt{2\xi_{5}, 9N_{9}}}{\sqrt{2\xi_{5}, 9N_{9}}} = \frac{\sqrt{2.11.7 \times 8.65 \times 10^{-19} \cdot 1.6 \times 10^{-19} \times 3 \times 10^{17}}}{3.83 \times 10^{-7}} = 0.82 \text{ V}^{2}$ Depletion: Vog TOTUM b) Ital charge: Qs = - 9. NA NA = -2x6 c/22 Φος = Ε. × to× = 0.54 × 6,03×10 9×10 c nd = 0 Φ<sub>5</sub>≥0 Electric field: $\frac{-1.75 \times 6^{-7}}{3.9 \times 6.85 \times 10^{-17}} = -2.24 \times 10^{6} \text{ V/cm}$







V > Ju => diplition.

Cs =  $\frac{9}{2kt}$  Cox (VFB-V) = 1.49 × 10 F/c2 77 Cox

 $C_{LP} = C_{HF} = \left(\frac{1}{\cos x} + \frac{1}{c_s}\right)^{-1} = 3.73 \times 10^{-3} P/\omega^2 \simeq C_{OX}$ 

 $\Phi_{S} = \frac{PN_{A}N_{A}}{2(E_{S})} = 0.63v$   $Q_{S} = -9. N_{A}N_{A} = -2.5 \times 10^{-7} \text{ C/c}^{2}$   $E_{OX} = -\frac{Q_{S}}{E_{OZ}} = 1.23 \times 10^{J} \text{ V/cm}$   $C_{LF} = C_{HF} = \frac{C_{OX}}{\sqrt{1 + \frac{4(v - \sqrt{F_{S}})}{2}}} = 1.3 \times 10^{-7} \text{ F/cm}^{-7}$ 

other hand, holes in SiO<sub>2</sub> have an extremely small mobility (<10<sup>-8</sup> cm<sup>2</sup>/Vs at room temperature) and eventually a fraction of the radiation-induced holes will be trapped at the oxide-semiconductor interface, acting as a sheet of fixed charges. a) Consider a MOS (metal/SiO<sub>2</sub>/p-Si) structure, with an oxide thickness of 25 nm, subjected to ionizing radiation. Assume that, during the exposure to radiation,  $10^{18}$ electron-hole pairs/cm<sup>3</sup> are created in the oxide. Assume also that all electrons are removed from the oxide without recombining with the radiation-induced holes, and that 20% of the generated holes are trapped at the oxide-semiconductor interface. Will the threshold voltage  $V_{th}$  increase or decrease after irradiation? Provide an estimation of the change in  $V_{th}$ . b) Repeat point a) but considering oxide thicknesses of 12 nm and 8 nm. What can we conclude about the radiation resistance of MOS device? Do you think a power MOSFET (=a MOSFET for power electronics applications, with a thick gate oxide) will be more or less resistant to radiation than a MOS device for logic applications

4. An ideal MOSFET with p-Si substrate has the following parameters: SiO2 gate oxide thickness = 8 nm, inversion channel mobility  $\mu_n = 450 \text{ cm}^2/\text{Vs}$ , and threshold voltage  $V_{th}$ = 0.4 V. The measured current in the saturation region is  $I_{D.sat}$  = 0.8 mA when biased at  $V_{gs} = 2.0 \text{ V}.$ a) Determine the width-to-length (W/L) ratio. b) Consider now an ideal MOSFET with n-Si substrate, with the same oxide thickness

as above, with a mobility of  $\mu_p = 210 \text{ cm}^2/\text{Vs}$ , and a threshold voltage of  $V_{th} = 0.4$ V. The measured current in the saturation region is also  $I_{D,sat} = 0.8$  mA when biased at  $V_{sq} = 2.0$  V. Determine the W/L ratio in this case. Which of the two devices (n-channel and p-channel MOSFET) you think enables a lower device size?

biased under reverse voltage V. a) Calculate the expression of the maximum voltage (breakdown voltage) V<sub>br</sub> that can be applied to the structure, and the specific ON-Resistance R<sub>ON,sp</sub> of the drift layer, and describe the assumptions that were be made to simplify their determination. Which material properties affect them? b) Correlate the breakdown Voltage V<sub>br</sub> and the specific ON-resistance R<sub>ON,sp</sub> of the

5. Consider a p-i-n structure, with an intrinsic (drift) region of thickness WD and doping ND,

(with a thin gate oxide)?

c) How can you have both a high V<sub>br</sub> and a low R<sub>on</sub>? Why is this important for power

d) If instead of a power device, you wanted to make radio frequency (RF) devices?

What would be the main parameters for high performance devices?